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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,879	07/15/2003	Eric N. Paton	039153-0647 (H0976)	7815

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EXAMINER	
LE, THAO P	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 03/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,879	PATON ET AL.	
	Examiner	Art Unit	
	Thao P Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 7/15/03 is acceptable.

2. Claims 1-20 are pending in this application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denning et al., U.S. Patent No. 6,187,682 in view of Okuno et al., U.S. Patent No. 6,486,520.

Regarding to claim 1, Denning et al. discloses a method of manufacturing an integrated circuit (IC) similar to what recited in claim 1. See Figs. 1-7 and Cols. 1-12. Denning et al. discloses the method of manufacturing an IC comprising:

. providing a substrate 102 (Fig. 5), the substrate including germanium (substrate 102 is major portion of wafer 26 which is formed of silicon, germanium, or germanium silicon, lines 65-67, Col. 7; lines 40-44, Col. 4),

. providing a gate structure 112 (Fig. 5) above the substrate,

. pre-cleaning the substrate (lines 13-22, Col. 8) with an argon and hydrogen plasma (lines 5-6, Col. 3; lines 59-65, Col. 4), and

. siliciding the substrate 120 (Fig. 7) (lines 35-40, Col. 8).

However, Denning et al. fails to disclose the substrate includes a layer containing germanium.

Okuno et al. discloses a method of forming an integrated circuit comprising the step of forming a substrate 20 whereas the substrate 20 includes a germanium layer 52 formed thereon (**Figs. 7-9; Abstract**).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Denning et al. as taught by Okuno et al. by forming a germanium layer 52 on the substrate because germanium material would increase capacitance of dielectric films, prevent formation of a low dielectric constant layer between the gate dielectric and the semiconductor substrate (Okuno et al., Abstract), in addition, germanium is well known to have high carrier mobility (e.g, high hole and electron mobility) and optical absorption as compared to silicon. That is why germanium film is useful for devices that require enhanced performance and/or high

quantum efficiency. Those devices such as MOS transistors would benefit from the use of germanium film.

Regarding to claim 2, Denning et al. and Okuno et al. disclose the claimed limitations as applied to claim 1 above, and Denning et al. further discloses the pre-cleaning process utilizing a hydrogen argon plasma (lines 5-6, Col. 3; lines 59-65, Col. 4).

Regarding to claim 5, Denning et al. and Okuno et al. disclose the claimed limitations as applied to claim 1 above, Denning et al. further discloses the gate structure includes a polysilicon conductor 112 (Figs. 5-7) (line 7, Col. 8).

Regarding to claim 6, Denning et al. and Okuno et al. disclose the claimed limitations as applied to claims 1 and 5 above, Denning et al. further discloses the polysilicon conductor 112 is pre-cleaned and silicided 120 (Fig. 7) (lines 5-40, Col. 8).

5. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denning et al., U.S. Patent No. 6,187,682 in view of Okuno et al., U.S. Patent No. 6,486,520, and further in view of Moslehi, U.S. Patent No. 5,403,434.

Regarding to claims 3-4, Denning et al. and Okuno et al. discloses all claimed limitations as applied to claim 1 above except for the steps of utilizing an HF dip (claim 3) and exposing the substrate to a wet bath (claim 4) in the pre-cleaning process.

Moslehi discloses the conventional procedure for removing native oxides in pre-cleaning process including the step of using wet cleaning containing HF dip or HF wet bath and exposing the substrate to the HF wet bath (lines 50-60, Col. 1).

It would have been obvious to one having ordinary skill in the art to use wet clean as cited in Moslehi and then plasma clean as disclosed in Denning in pre-cleaning process to remove native oxides **because** the wet clean follow by plasma clean before depositing materials on the substrate would reduce contact resistance, improve uniformity and conductivity, and reduce the manufacturing cost. The wet clean removes contaminants and most of native oxides at a lower cost and faster process but doesn't remove the native oxides that grow when the substrate is exposed to the air due to ambient exposure during wafer transport from the wet clean bath to the fabrication equipment (Moslehi, lines 50-60, Col. 1; lines 10-14, Col. 2), meanwhile, plasma clean (require higher cost and slower process) disclosed in Denning et al. using the same chamber for both plasma cleaning and depositing film would remove all native oxides that grow when the substrate is exposed to the air to avoid adversely effect subsequent processing steps, for example, causing high contact resistance or impeding interfacial reactions of films deposited on the substrate materials.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 7, 12-16 are rejected under 35 USC 102 (b) as being anticipated by Denning et al., U.S. Patent No. 6,187,682.

Regarding to claim 7, Denning et al. discloses a method of pre-cleaning a top surface of an IC substrate before silicidation in a chamber similar to what recited in claim 7. See Figs. 1-7 and Cols. 1-12. Denning et al. discloses the method of pre-cleaning a top surface of an IC substrate before silicidation in a chamber comprising:

. providing a plasma including hydrogen in the chamber (Figs. 1-4, lines 5-6, Col. 3; lines 59-65, Col. 4),

. removing native oxide from the IC substrate (lines 10-12, Col. 3; lines 57-60, Col. 5; lines 45-50, Col. 6).

Regarding to claim 12, Denning et al. further discloses a step of providing a silicide layer 120 (Fig. 7) (lines 35-40, Col. 8).

Regarding to claim 13, Denning et al. discloses a step of evacuating the chamber (lines 51-52, Col. 4).

Regarding to claim 14, Denning et al. discloses the plasma includes argon (lines 59-60, Col. 4).

Regarding to claim 15, Denning et al. discloses the IC substrate includes a germanium (lines 40-43, Col. 4) containing gate conductor 112 (Fig. 5) (lines 7-9, Col. 8).

Regarding to claim 16, Denning et al. discloses the chamber is part of a deposition tool (Figs. 1-3, lines 1-30, Col. 3).

8. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denning et al., U.S. Patent No. 6,187,682 in view of Moslehi, U.S. Patent No. 5,403,434.

Regarding to claims 8-9, Denning et al. discloses all claimed limitations as applied to claim 7 above but fails to disclose wherein the method above further

comprising the step of exposing the substrate to a wet bath to reduce a thickness of the native oxide (claim 8) and wherein the wet bath utilizes HF (claim 9).

In the other hand, Moslehi discloses the conventional procedure for removing most but not all native oxides to eliminate the thickness of native oxides on the substrate in pre-cleaning process using wet cleaning containing HF dip or HF wet bath (lines 50-60, Col. 1).

It would have been obvious to one having ordinary skill in the art to use wet clean as cited in Moslehi in addition of plasma clean as disclosed in Denning in pre-cleaning process to remove native oxides **because** the wet clean follow by plasma clean before depositing films on the substrate would reduce contact resistance, improve uniformity and conductivity, and reduce the manufacturing cost. The wet clean removes contaminants and most of native oxides at a lower cost and faster process but doesn't remove the native oxides that grow when the substrate is exposed to the air due to ambient exposure during wafer transport from the wet clean bath to the fabrication equipment (Moslehi, lines 50-60, Col. 1; lines 10-14, Col. 2), meanwhile, plasma clean (higher cost and slower process) disclosed in Denning et al. using the same chamber for both plasma cleaning and depositing film removes all native oxides that grow when the substrate is exposed to the air to avoid adversely effect subsequent processing steps, for example, causing high contact resistance or impeding interfacial reactions of films deposited on the substrate materials.

Regarding to claim 10, Denning et al. discloses all limitations as applied to claim 7, Denning et al. and and Moslehi disclose all claimed limitations as applied in claim 8 above, and Denning et al. further discloses the chamber is a vacuum chamber and a metal layer 116 (Fig. 6) is deposited on the IC substrate in the chamber after the pre-clean step (lines 13-50, Col. 8).

Regarding to claim 11, Denning et al. discloses all limitations as applied to claim 7, Denning et al. and Moslehi disclose all claimed limitations as applied to claims 8 and 10 above, and Moslehi further discloses the conventional cleaning process to eliminate the thickness of native oxides on the substrate using wet bath (lines 50-55, Col. 1). It is inherent that removing native oxides off the substrate using wet bath as taught in Moslehi would eliminate the thickness of native oxides on the substrate.

9. Claim 17 is rejected under 35 USC 102 (b) as being anticipated by Denning et al., U.S. Patent No. 6,187,682.

Regarding to claim 17, Denning et al. discloses a method of manufacturing a transistor on an integrated circuit (IC) similar to what recited in claim 17. See Figs. 1-7 and Cols. 1-12. Denning et al. discloses the method of manufacturing a transistor on an IC comprising:

. providing a gate structure 112 (Fig. 5) on a top surface of a strained silicon layer or a silicon germanium layer 102 (lines 65-67, Col. 7; lines 40-44, Col. 4),

. providing a plasma including an argon and hydrogen (lines 5-6, Col. 3; lines 59-65, Col. 4) to remove a native oxide material (lines 10-12, Col. 3; lines 57-60, Col. 5; lines 45-50, Col. 6),

. siliciding the top surface 120 (Fig. 7) (lines 35-40, Col. 8).

10. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denning et al., U.S. Patent No. 6,187,682 in view of Moslehi, U.S. Patent No. 5,403,434.

Regarding to claim 18, Denning et al. discloses all claimed limitations as applied to claim 17 above but fails to disclose the step of utilizing HF acid to remove a portion of the native oxide material before providing the plasma clean including hydrogen and argon.

Moslehi discloses the conventional procedure for removing most but not all native oxides in pre-cleaning process using wet cleaning containing HF acid.

It would have been obvious to one having ordinary skill in the art to use wet clean as cited in Moslehi and then use plasma clean as disclosed in Denning in pre-cleaning process to remove native oxides **because** the wet clean follow by plasma clean before depositing film on the substrate would reduce contact resistance, improve uniformity and conductivity, and reduce the manufacturing cost. The wet clean removes contaminants and most of native oxides at a lower cost and faster process but doesn't

remove the native oxides that grow when the substrate is exposed to the air due to ambient exposure during wafer transport from the wet clean bath to the fabrication equipment (Moslehi, lines 50-60, Col. 1; lines 10-14, Col. 2), meanwhile, plasma clean (higher cost) disclosed in Denning et al. using the same chamber for both plasma cleaning and depositing film removes all native oxides that grow when the substrate is exposed to the air to avoid adversely effect subsequent processing steps, for example, causing high contact resistance or impeding interfacial reactions of films deposited on the substrate materials.

Regarding to claim 19, Denning et al. discloses all claimed limitations as applied to claim 17, Denning et al. and Moslehi disclose all claimed limitations as applied to claim 18, and Denning et al. further discloses the siliciding is a nickel siliciding process (lines 25-28, Col. 4; lines 65-67, Col. 10).

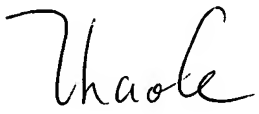
Regarding to claim 20, Denning et al. discloses all claimed limitations as applied to claim 17, Denning et al. and Moslehi disclose all claimed limitations as applied to claims 18 and 19, and Denning et al. further discloses the top surface includes a germanium (Denning et al., wafer 26 containing silicon/germanium, lines 40-43, Col. 4) containing gate conductor 112 (Fig. 5).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1956.



Thao Phuong Le

Examiner